Power Management Unit with DCDC Controller

Check for Samples: TPS659110, TPS659112, TPS659113

FEATURES

The purpose of the TPS659110 device is to provide the following resources:

- **Embedded power controller (EPC) with EEPROM programmability**
- **Two efficient step-down DCDC converters for processor cores (VDD1, VDD2)**
- **One efficient step-down DCDC converter for I/O power (VIO)**
- **One controller for external FETs (VDDCtrl)**
- **Dynamic voltage scaling for processor cores**
- **Eight LDO voltage regulators and one RTC LDO (supply for internal RTC)**
- **One high-speed I^2C interface for general-purpose control commands (CTL-I^2C)**
- **Two independent enable signals for controlling power resources (EN1, EN2). Alternatively, these pins can be used as a high-speed I^2C interface dedicated for voltage scaling for VDD1 and VDD2.**
- **Thermal shutdown protection and hot-die detection**
- **A real-time clock (RTC) resource with:**
  - **Oscillator for 32.768-kHz crystal or 32-kHz built-in RC oscillator**
  - **Date, time and calendar**
  - **Alarm capability**
- **Nine configurable GPIOs with multiplexed feature support:**
  - **Four can be used as enable for external resources, included into power up sequence and controlled by state-machine.**
  - **As GPI, GPIOs support logic-level detection and can generate maskable interrupt for wake-up.**
  - **Two of the GPIOs have 10 mA current sink capability for driving LEDs.**
  - **DCDCs switching synchronization through an external 3-MHz clock.**
- **Two reset inputs, for cold reset (HDRST) and a power initialization reset (PWRDN) for thermal reset input**
- **32-kHz clock and reset (NRESPWRON) for system and an additional output for reset signal**
- **Watchdog**
- **Two ON/OFF LED pulse generators and one PWM generator**
- **Two comparators for system control, connected to VCCS pin**
- **A JTAG® and boundary scan, but not accessible in functional mode (test purpose)**

APPLICATIONS

- **Portable and handheld systems**

DESCRIPTION

The TPS659110 is an integrated Power Management IC available in 98-pin 0.65-mm pitch BGA package and dedicated to applications powered by one Li-Ion or Li-Ion polymer battery cell or 3-series Ni-MH cells or a 5 V input, and which require multiple power rails. The device provides three step-down converters, one controller for external FETs to support high current rail, eight LDOs, and is designed to be flexible PMIC for supporting different processors and applications.

Two of the step-down converters provide power for dual processor cores and support dynamic voltage scaling by a dedicated I^2C interface for optimum power savings. The third converter provides power for the I/Os and memory in the system.

The device includes eight general-purpose LDOs providing a wide range of voltage and current capabilities. Five of the LDOs support 1.0 to 3.3 V with 100-mV step and three (LDO1, LDO2, LDO4) support 1.0 to 3.3 V with 50-mV step. All LDOs are fully controllable by the I^2C interface.

In addition to the power resources, the device contains an EPC to manage the power sequencing requirements of systems and an RTC. Power sequencing is programmable by EEPROM.

Figure 1 shows the top-level diagram of the device.

PRODUCT PREVIEW

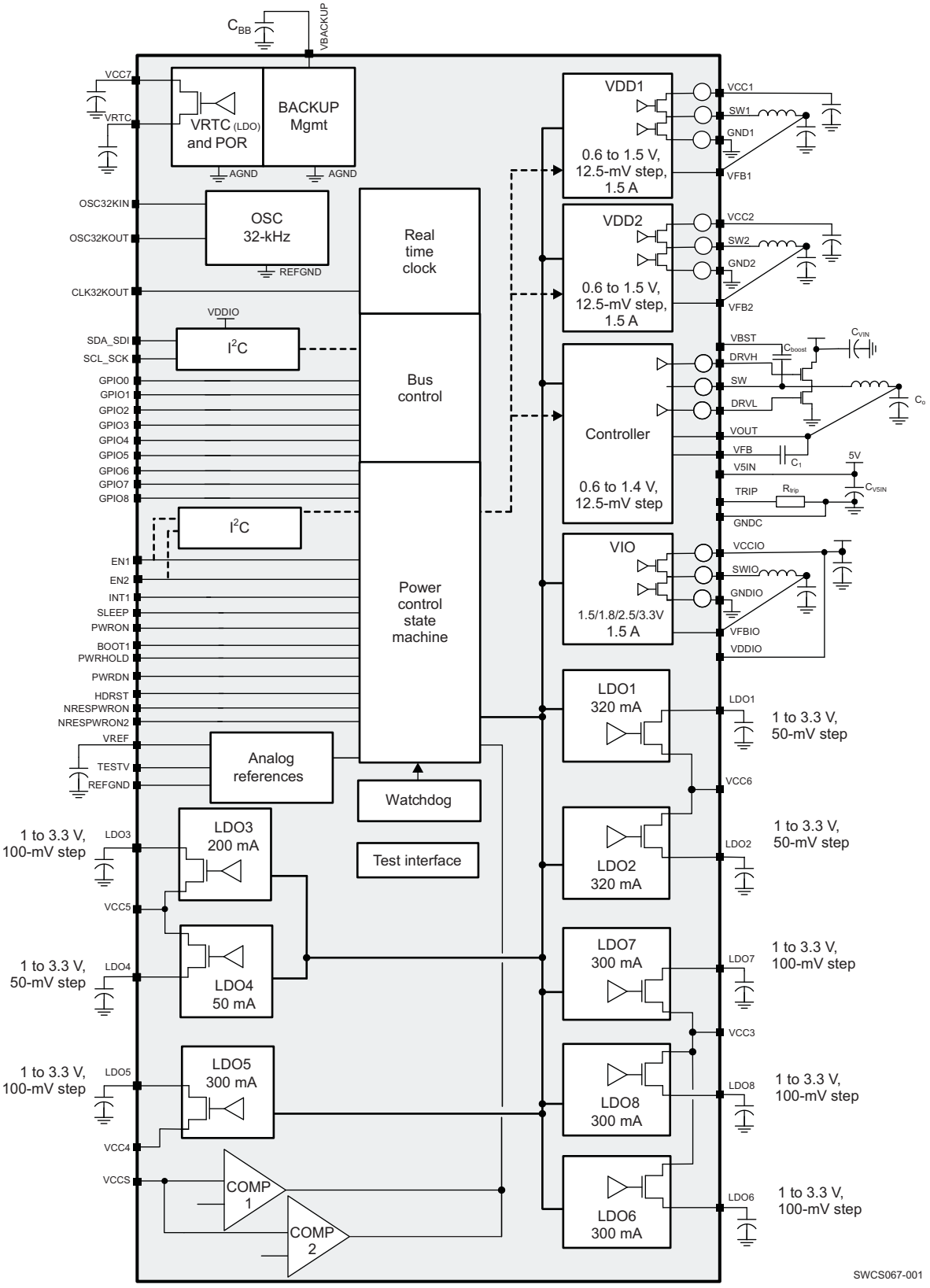


Figure 1. Top-Level Diagram

Table 1. ORDERING INFORMATION

Part Number	Ordering	Memory Support (DDR3/LPDDR2)	Processors
TPS659110(1)	PTPS6591102A2ZRC/R	LPDDR2	NVIDIA T30
	PTPS6591104A2ZRC/R	DDR3	NVIDIA T30
TPS659112	PTPS659112A2ZRC/R	N/A	DM8168, DM8167, C6A8168, C6A8167, AM3894, AM3892
TPS659113	PTPS659113A2ZRC/R	N/A	DM8148, DM8147, DM8146, C6A8148, C6A8147, C6A8143, AM3874, AM3872, AM3871

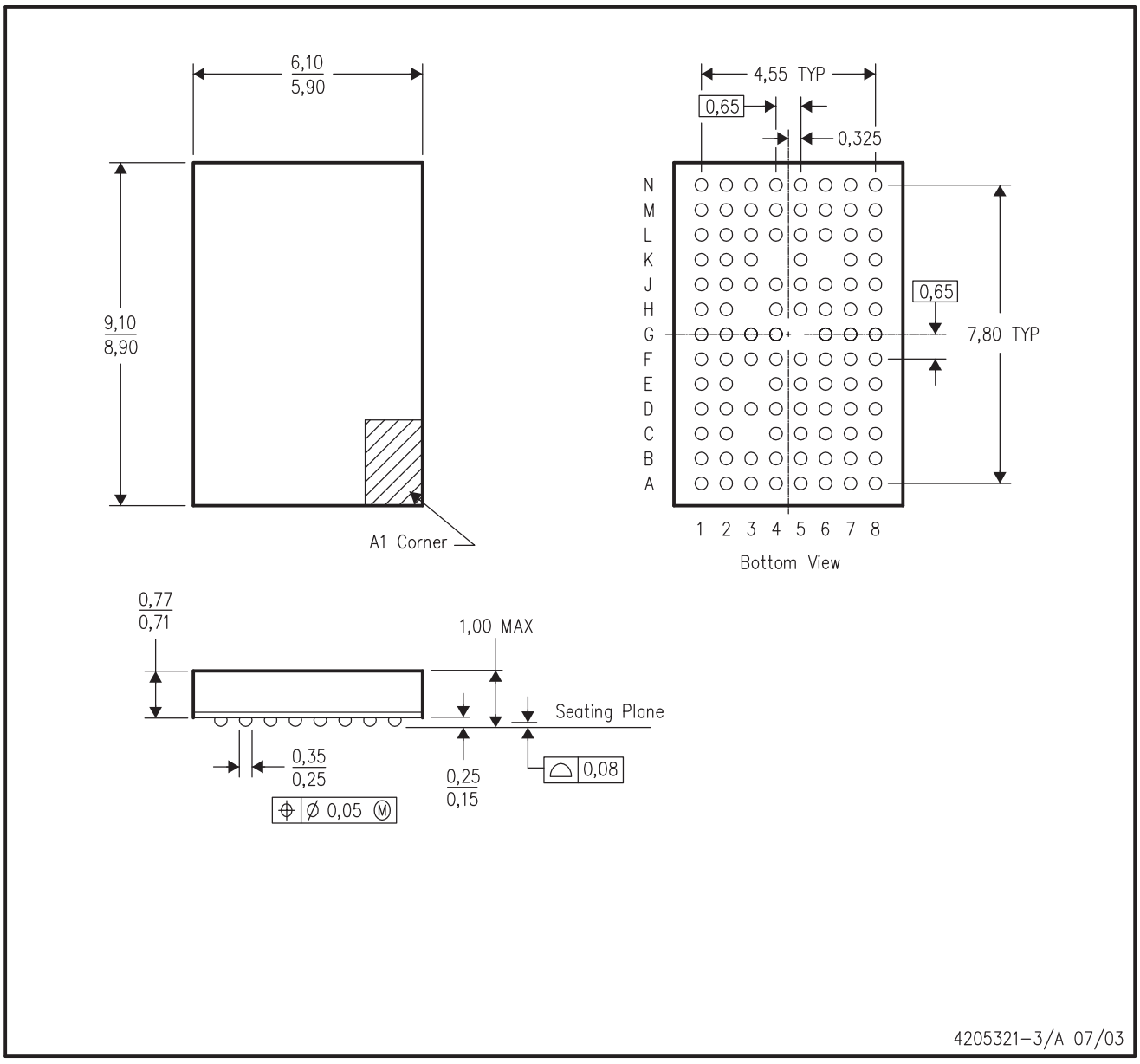
(1) For various part numbers, contact your TI representative.

PRODUCT PREVIEW

For the complete TPS65911 data sheet, contact your TI sales representative. The document is internally available for download on ESP under the corresponding TPS659110/2/3 product folders and can be shared with customers.

PACKAGE MECHANICAL DATA

ZRC (S–PBGA–N98) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

SWCS067-002

Figure 2. Package Mechanical Data

PRODUCT PREVIEW

PACKAGING INFORMATION

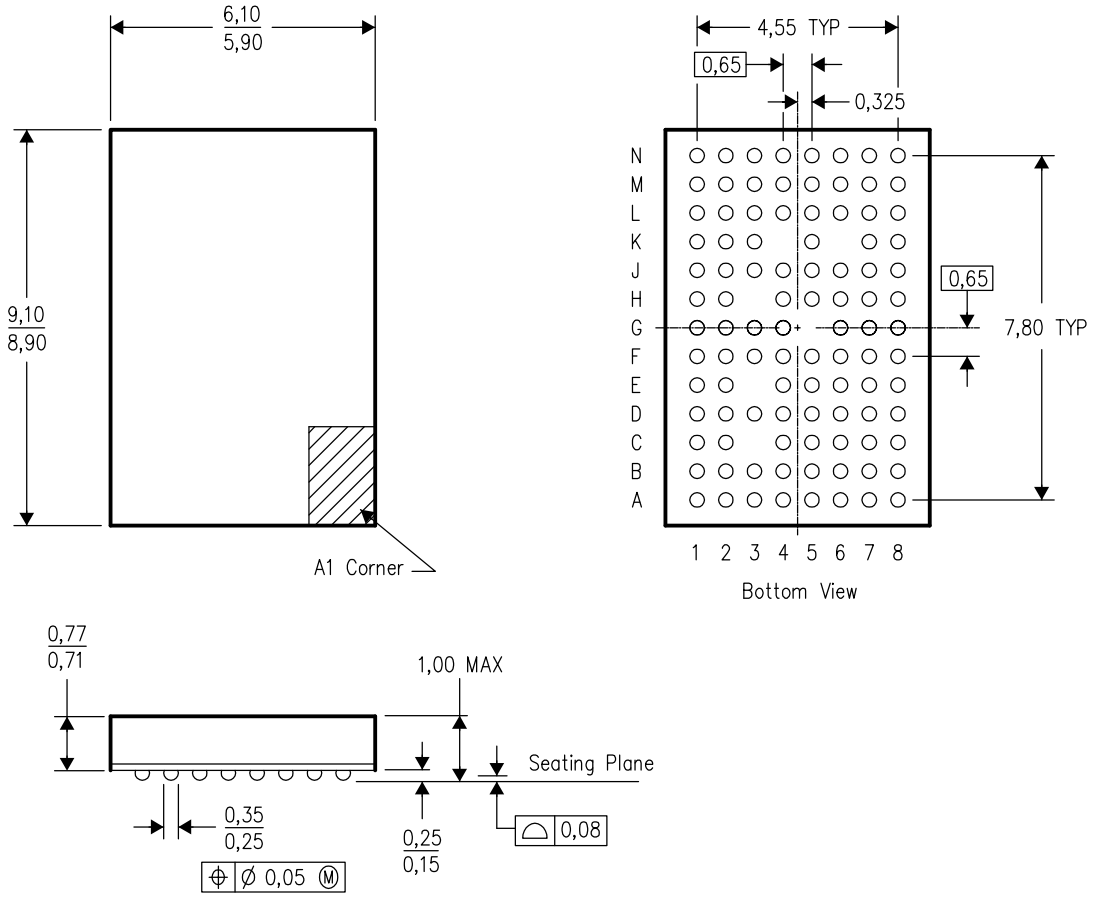
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS659110A2ZRC	PREVIEW	BGA MICROSTAR JUNIOR	ZRC	98	240	Green (RoHS & no Sb/Br)	CUNIAU	Level-3-260C-168 HR	
TPS659110A2ZRCR	PREVIEW	BGA MICROSTAR JUNIOR	ZRC	98	2500	Green (RoHS & no Sb/Br)	CUNIAU	Level-3-260C-168 HR	
TPS659112A2ZRC	PREVIEW	BGA MICROSTAR JUNIOR	ZRC	98	240	Green (RoHS & no Sb/Br)	CUNIAU	Level-3-260C-168 HR	
TPS659112A2ZRCR	PREVIEW	BGA MICROSTAR JUNIOR	ZRC	98	2500	Green (RoHS & no Sb/Br)	CUNIAU	Level-3-260C-168 HR	
TPS659113A2ZRC	PREVIEW	BGA MICROSTAR JUNIOR	ZRC	98	240	Green (RoHS & no Sb/Br)	CUNIAU	Level-3-260C-168 HR	
TPS659113A2ZRCR	PREVIEW	BGA MICROSTAR JUNIOR	ZRC	98	2500	Green (RoHS & no Sb/Br)	CUNIAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZRC (S–PBGA–N98) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

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